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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
3663	

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,022	YU, TA-LEE	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32,33,35,37,38 and 47-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32,33,35,37,38 and 47-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *3/2/04* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination ("RCE") under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/27/06 has been entered.

Response to Amendment

Amendment filed 4/27/06 with said REC forms the basis for this office action. Applicant substantially amended claims 32-33, 35, 37-38 and 47-48 through substantial amendment of the independent claim 32, 33 and 37, and substantially amended claims 49-55 through substantial amendment of independent claim 49 and claims 50-53 and 55. Examiner wishes to make of record that an incorrect serial number (10/666,493) features in said Amendment to the claims and the accompanying Remarks although the correct serial number (10/791,022) identifies the submission through the cover letter.

Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

Drawings

The drawings are objected to under 37 CFR 1.83(b) because they are incomplete. 37 CFR 1.83(b) reads as follows:

> When the invention consists of an improvement on an old machine the drawing must when possible exhibit, in one or more views, the improved portion itself, disconnected from the old structure, and also in another view, so

much only of the old structure as will suffice to show the connection of the invention therewith.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action.

In particular, the illustration of the invention is incomplete through failure to identify the claimed multiple bipolar transistors in cross-sectional view, for which several different options of identification offer themselves in light of Figures 2, 3 and 5D. Specifically, any combination of emitter, base and collector region forms a bipolar transistor when abutting (npn).

The objection to the drawings will not be held in abeyance.

Claim Objections

1. ***Claims 32-33, 35, 37-38 and 47-48*** are objected to because of the following informalities: the wording "a top one of one said first regions and" in claim 32, line 24 should be replaced by "a first one of said first regions"; furthermore, the wording "a bottom one of said first regions" in claim 32, line 25 should be replaced by "a second one of said first regions, said first one and said second one of said first regions being located on laterally opposite ends of the semiconductor substrate".

   Appropriate correction is required.

2. ***Claims 49-55*** are objected to because of the following informalities: the wording "a top one of one said first regions and" in claim 49, line 23, should be replaced by "a first one of said first regions"; furthermore, the wording "a bottom one of said first regions" in claim 49, line 24 should be replaced by "a second one of said first regions, said first one and said second one of said first regions being located on laterally opposite ends of the semiconductor substrate".

   Appropriate correction is required.

3. ***Claims 32-33, 35, 37, 38 and 47-48*** are objected to because of the following informalities: the wording "with "N" number of said third regions, whereby "N" is the number of multiple bipolar transistors" (claim 32, lines 20-21) should be replaced by: "wherein each of said third regions stands in a one-to-one relation with a bipolar transistor comprising one of said first regions thus forming electrically parallel multiple bipolar transistors".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. ***Claims 32-33, 37-38, 47, 49-50 and 52-54*** are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al.

On claim 32: Chen et al teach (Figure 4, title, abstract, and cols. 1-5) an integrated vertical multiple npn transistor ESD protection structure on a semiconductor substrate 42 (col. 3, l. 35-36) (title and abstract; Figure 4 and cols. 2-4), functionally connected between an integrated circuit input or output pin 34 (col. 3, l. 5) and ground (indicated in Figure 4) which will prevent electrostatic discharge damage to said integrated circuit comprising;

a (N+ type) first semiconductor layer 44 (col. 3, l. 35) having a first conductivity dopant type (N-type);

a (N type) second semiconductor layer (central Nwell portion of 46) (col. 3, l. 40-42) overlying said (N+ type) first semiconductor layer, having a similar conductivity type as said first layer, but a different dopant concentration (N instead of N+);

a (P type) third semiconductor layer 62 (col. 3, l. 62) having a second conductivity dopant type opposite that of said first semiconductor layer (P-type), disposed in overlying relation to said second semiconductor layer (cf. Fig. 4);

a plurality of first (N+ type) regions (50 and abutting remnant of 46 separated from Nwell 46 to the outside of 50; see Figure 4) (col. 3, l. 47-50) of said first conductivity type (N-type) electrically connecting with said (N+ type) first semiconductor layer, having a top element 58 (col. 3, l. 59) making electrical contact to said first regions and said (N+ type) first semiconductor layer (col. 3, l. 55-59);

a plurality of (P+ type) second regions 64 and 56 (col. 3, l. 53-60 and 63) of said second conductivity dopant type (P-type) laterally spaced from said (N+ type) first regions (cf. Fig. 4), being electrically connected to said (P type) third semiconductor layer having a top element 76 making electrical contact to said (P+ type) second regions and said (P type) second semiconductor layer (see Figure 4);

a plurality of (second N+ type) third regions 66 (col. 4, l. 4) of said first semiconductor layer conductivity dopant type (N-type) laterally spaced and interposed between said second regions,

wherein said (second N+ type) third regions 66 are alternatingly arranged in an array within said (P type) third semiconductor layer , wherein the number of said (second N+ type) third regions is equal to the number of multiple bipolar transistors (hence each in an electrically parallel array that comprise said ESD structure, and wherein one of said second regions of said second conductivity dopant type is disposed between said array and a top one of said first regions and another of said second regions is disposed between said array and a bottom one of said first regions, wherein "top" and "bottom" refer to lateral end portions of the structure on said semiconductor substrate.

In conclusion, Chen et al anticipates claims 32 and 49.

On claims 33 and 50: the plurality of (N+ type) first regions 50 (+remnant of Nwell 46 as defined above) together with the associated connected (N+ type) first semiconductor layer 44 are with N dopant and form multiple collector elements of a bipolar transistor in which the bases are formed by said (P-type) third semiconductor layer 62 and associated with said plurality of the P+ type regions, and by which multiple emitter elements are formed by said plurality of laterally spaced (second N+ type) third regions 66 of N type dopant (cf. Figures 4 and 6: N.B. 65 are the emitter contacts (col. 3, l. 64)).

*On claims 35 and 51:*said first regions (50 and remnant of Nwell 46) have horizontal contact conductor stripes Upper surfaces of 50) at the top and bottom of said transistor array ("top" and "bottom" again interpreted as being on opposite end portions laterally) which are ultimately connected together (through wires 58) and to a first voltage source on the integrated circuit (said horizontal conductor stripes being N+ regions 50).

On claims 37 and 52: the third regions 66 are electrically connected by a conductor element with horizontal stripe conductor elements, for each element of the array holding N elements (see definition as implicit in amended claim language of claims 32 and 49, respectively) in total, there is one aforementioned horizontal stripe conductor element (indented, lower plateau portion of polysilicon 68 (col. 4, l. 5) and connected in a contiguous (otherwise no voltage could be sustained and no current could flow) and box-shape manner by contact conductor elements with vertical

extension (see Figure 4: elements 68, loc.cit.), hence qualifying as "vertical contact conductor elements", at both ends of said horizontal emitted conductor stripes and lower plateau and vertical extension indeed forming a box shape (see Figure 4).

On claims 38, 47, 53 and 54: the plurality of the (or, in the alternative: said) (P+ type) second regions 64 and 56 and said (second N+ type) third regions 66 are ultimately connected together (see wire 60 from 66/65 through connected to 56 and connected through wire 76 to 64) (Figure 4) and to a second voltage source that is ground (claims 47 and 54 are thus also met).

On claims 48 and 55: the (second N+ type) third regions 66 are electrically connected by a conductor element 68 (col. 4, l. 5) with N horizontal stripe conductor elements (each horizontal strip being indented portion of 68 positioned lower than a high-level plateau (see Figure 4)), and at least two of the horizontal stripe conductor elements are connected by at least one first vertical contact conductor element (contact between 68 and 66) (Figure 4) at one end of the horizontal stripe conductor elements (bottom end of the far left end of array 66 in Figure 4), and at least two of the horizontal stripe conductor elements are connected by at least one second vertical contact conductor element at another end of the horizontal stripe conductor elements (bottom end of the far right end of array 66 in Figure 4) so that the horizontal stripe conductor elements are connected to each other.

Response to Arguments

Applicant's arguments filed 4/27/06 have been fully considered but they are not persuasive. In particular, the currently amended language of claim 32 appears to read

on the elected invention (Figure 5D; see the Response filed on 3/5/03 to the Restriction/Election Requirement mailed 1/29/03 in the parent application 10/266,665).

(1) With regard to the traverse of the objection to the Drawings, reference in the claims is made to a third semiconductor layer (24) overlying said first semiconductor layer (12), implicitly defining a vertical direction different from the one inherent in the recited top and bottom ones of said first regions (16). It appears from applicant's comments in traverse that what applicant means, with top and bottom first regions, is first and second ones of said first regions on laterally opposite ends of the semiconductor substrate. The objection to the Drawings is herewith withdrawn.

(2) With regard to the traverse of the rejection under 35 USC 112, first paragraph, of claims 32-33, 35, 37-38 and 47-48:

The remedy implemented by applicant is still problematic because the limitation: "with "N" number of said third regions", does not define "N". Does Applicant mean "wherein, when "N" by definition is the number of said third regions"? Then Applicant should claim this. But without said definition the subsequent limitation "whereby "N" is the number of multiple bipolar transistors" defines "N", and the limitation preceding said subsequent limitation then logically must mean that said number of bipolar transistors is equal to the number of third regions 26. However, no interpretation consistent with claim 32 is also consistent with Figure 5D of the elected invention. Disclosed is a set of npn junctions, said set forming multiple bipolar transistors. However, the number of npn junctions in said set is not equal to the number of third regions (26 positioned directly underneath 28 as shown in Figure 5D; see Figure 2). Because the emitter is contiguous

and the base contacts and collector contacts are short-circuited, electrically there is only one bipolar transistor (emitter-base-collector). Interpreting "bipolar transistor" to mean "npn junction", then the number of bipolar transistors in Figure 5D is at least eight (8) (with reference to Figure 5D, any horizontal portion of 28B in Figure 5D forms a npn junction with both the upper and lower base and collector contacts), but the number of said third regions 26 is only four (4). From applicant's Remarks examiner believes that applicant means by "bipolar transistor" an npn junction associated specifically with an emitter region and a given collector region the latter being fixed when counting the number of bipolar transistors. An objection is provided to remove the above problems with terminology.

(B) With regard to Applicant's traverse of the rejection of claims 49 and dependent claims under 35 USC 112, first paragraph, applicant's argument of traverse is based on the combination of two figures, i.e., a cross sectional view (Figure 2) showing semiconductor layer 14 *overlying* said first conductivity layer 12 and a plan view (Figure 5D), showing *top and bottom* ones of said first regions 18; however, the vertical direction inherent in the description of said *overlying* is perpendicular to the vertical direction inherent in the description of top and bottom of said first regions. An objection is issued to remedy the problem under the assumption that by "top" and "bottom" applicant means the locations on laterally opposite sides of the semiconductor substrate, i.e., in cross-sectional view.

(C) *The rejection under 35 USC 112, second paragraph* of ad sections 5 and 6 on page 5 of the previous office action have been withdrawn given persuasive arguments by applicant based on the current claim amendment.

(D) *The rejection under 35 USC 112, second paragraph, of claims 37 and 52 (claim 36 should indeed have been claim 37, with thanks to applicant) has been successfully overcome* by the amendment to claim 37.

(E) With regard to the traverse of the rejection under 35 USC 102(b) of claims 32-33, 38-38, 47-50 and 52-55 ,

(E-1) The first argument on page 9 (in particular: second paragraph; the first paragraph merely stating properties of the device by Chen et al) is that "Applicant's claimed invention does not require the additional devices to assure uniform turn on of multiple emitter fingers", reducing "design and processing requirements" over Chen et al and leading to "a simpler, unique concept with less (i.e., fewer) overall components". However, the argument is not persuasive because *absence* of any additional devices does not persuasively traverse the rejection, based as the latter is on the *presence* of limitations in the device by Chen et al.

(E-2) The second argument by applicant (page 9, third paragraph) is based on an allegation of unique emitter shape. However, the argument is not persuasive because applicant does not identify where the claim language distinguishes applicant's device from the device by Chen et al through said unique emitter shape.

(E-3) the third argument by applicant (page 9, fourth paragraph – page 10, second paragraph) is that the invention of applicant overcomes the drawback of the

prior art by using continuously connected and uniquely shaped emitters. However, this argument is not persuasive because in terms of contiguous connection of emitter regions applicant does not appear to distinguish from Chen et al at least in their teaching of the prior art (Figure 6).

(E-4) applicant's allegation (pages 10-11) that Chen et al teach away from the invention by teaching additional components is not persuasive, at least because said components are not claimed to be absent in the present invention. Furthermore, any teaching away should teach away from certain structural limitations as claimed, and no such teaching can be found in Chen et al.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM
July 8, 2006

Patent Examiner:

Johannes Mondt (Art Unit: 3663).